

WHAT IS CLAIMED IS:

1 1. A method of forming an integrated circuit comprising:
2 providing a first diffusion region, the first diffusion region a source/drain region
3 of a first transistor;
4 providing a second diffusion region, the second diffusion region a source/drain
5 region of a second transistor;
6 providing an isolation region between the first and second diffusion regions; and
7 selectively implanting a first channel stop implant region and a second channel
8 stop implant region in the isolation region, the first channel stop implant region separate from the
9 second channel stop implant region.

1 2. The method of claim 1 wherein the first channel stop implant region and
2 the second channel stop implant region define at least a portion of an isolation conductive path
3 between the first diffusion region and the second diffusion region.

1 3. The method of claim 2 wherein a separation distance between the first
2 channel stop implant region and the second channel stop implant region is chosen to control a
3 voltage threshold of an isolation region transistor, the isolation region transistor formed by the
4 first diffusion region, the second diffusion region, and the isolation region.

1 4. The method of claim 3 wherein when the separation distance between the
2 first channel stop implant and second channel stop implant is reduced, the threshold voltage is
3 increased.

1 5. The method of claim 2 further comprising a third diffusion region,
2 wherein the first channel stop implant region and the second channel stop implant region form at
3 least a part of an isolation conductive path between the first diffusion region, the second
4 diffusion region, and the third diffusion region.

1 6. The method of claim 5 wherein the third diffusion region is coupled to a
2 ground pad.

1 7. The method of claim 2 further comprising providing a field oxide region
2 over the isolation region.

1 8. The method of claim 7 further comprising providing a gate over the field
2 oxide region, wherein when a threshold voltage is applied to the gate, current flows in the
3 isolation conducive path.

1 9. The method of claim 7 wherein the first diffusion region, second diffusion
2 region, and isolation region form a isolation region transistor, and the isolation region transistor
3 is used in as an electro-static discharge protection device.

1 10. The method of claim 9 wherein the first diffusion region, second diffusion
2 region, and isolation region form a isolation region transistor, and the isolation region transistor
3 is used in a charge pump circuit.

1 11. A method of forming an integrated circuit comprising:
2 growing a pad oxide layer on a substrate;
3 growing a silicon nitride layer on the pad oxide;
4 etching a first isolation region and a second isolation region from the silicon
5 nitride layer and the pad oxide layer;
6 depositing a spacer oxide;
7 etching the spacer oxide to form a first opening and a second opening in the first
8 isolation region, and a third opening in the second isolation region;
9 implanting a first channel stop implant region in the first opening and a second
10 channel stop implant region in the second opening in the first isolation region, and a third
11 channel stop region in the third opening in the second isolation region;
12 removing the remaining spacer oxide;
13 growing a field oxide in the first isolation region and the second isolation region;
14 removing the silicon nitride layer;
15 depositing a polysilicon layer;
16 etching the polysilicon layer; and
17 implanting a plurality of diffusion regions.

1 12. The method of claim 11 wherein the etched polysilicon layer comprises a
2 first gate region over the first isolation region and a second gate region over the second isolation
3 region.

1 13. The method of claim 12 wherein the first channel stop region and the
2 second channel stop region form at least a part of an isolation conductive path between a first
3 diffusion region and a second diffusion region, wherein the first diffusion region and the second
4 diffusion region are two of the plurality of diffusion regions.

1 14. The method of claim 13 wherein the first diffusion region and the second
2 diffusion region are at least partly defined by the first isolation region, and the plurality of
3 diffusion regions further includes a third diffusion region and a fourth diffusion region, where
4 the third diffusion region and the fourth diffusion region are at least partly defined by the second
5 isolation region, and
6 wherein current flows between the first diffusion region and the second diffusion
7 region at a first threshold voltage, and between the third diffusion region and the fourth diffusion
8 region at a second threshold voltage, the first threshold voltage less than the second threshold
9 voltage.

1 15. A method of forming an integrated circuit comprising:
2 providing a first diffusion region, the first diffusion region a source/drain region
3 of a first transistor;
4 providing a second diffusion region, the second diffusion region a source/drain
5 region of a second transistor;
6 providing a third diffusion region;
7 providing an isolation region between the first, second and third diffusion regions;
8 and
9 selectively implanting a first channel stop implant region, a second channel stop
10 implant region, and a third channel stop implant region in the isolation region, the first channel
11 stop implant region, the second channel stop region, and the third channel stop region separate
12 from each other.

1 16. The method of claim 15 wherein the first channel stop implant region, the
2 second channel stop implant region, and the third channel stop implant region define at least a
3 portion of an isolation conductive path among the first diffusion region, the second diffusion
4 region, and the third diffusion region.

1 17. The method of claim 16 wherein a separation distance between the first
2 channel stop implant region and the second channel stop implant region is chosen to control a
3 voltage threshold of an isolation region transistor formed by the first diffusion region, the second
4 diffusion region, the third diffusion region, and the isolation region.

1 18. The method of claim 17 wherein the third diffusion region is coupled to a
2 ground pad.

1 19. The method of claim 17 further comprising:
2 providing a field oxide region over the isolation region.

1 20. The method of claim 19 further comprising:
2 providing a gate over the field oxide region, wherein when the threshold voltage
3 is applied to the gate, current flows among the first diffusion region, the second diffusion region,
4 and the third diffusion region.